

SCINTILLATOR PAD DETECTOR FRONT END ELECTRONICS DESIGN.

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DRAFT 2

Abstract

The front electronics designed to read out the LHCb Scintillator Pad Detector (SPD) is described in this note. After defining the detector features and reporting the relevant characteristics of the signal, the architecture of the read out system is presented. Analog signal processing is done on an ASIC which has also a digital part for control and calibration. Finally, synchronization and front end controls questions are commented.

1 SPD signal shape and electronics specifications

1.1 SPD signal shape

The signal shape to be processed at the SPD is obtained from a Monte Carlo simulation and experimental data [1],[2]. The starting point is the deposited energy, whose spectrum is given by GEANT [3] simulations and checked out on a test beam [4]. The basic physical process from the photon scintillation emission to the photoelectron conversion and amplification in the photomultiplier are described following closely the preshower pulse shape description in [1].

Briefly described, the signal to be read out is generated as follows. The scintillator, excited by the incoming particle, emits a number of photons. Those are captured by an helix-shaped shifting fiber which reemits at lower wavelength. This fiber is in turn connected to a clear fiber feeding the photomultiplier.

The simulation takes into account the following effects :

- Luminosity vs. deposited energy. The amount of produced photons is strictly proportional to the deposited energy. Birks' law effects are not taken into account since the scintillator saturation limit is far away.
- Scintillator excitation and desexcitation. The scintillator excitation and desexcitation time is taken into account using the correspondingly convoluted exponential distributions. Those times, however, will essentially contribute adding up an overall delay while their effect on signal spread is negligible, since they are sensibly smaller than the fiber desexcitation time.
- Photon capture by helix fiber. This is simulated by a probability factor for a photon being captured and reemitted. This factor is tuned to fit the data, provided by E.Gouchtchine: 15 measured photoelectrons in average for 12×12 cm pads and 30 for 4×4 cm. This small fraction of measured photoelectrons is essentially accounted by three effects, namely, the photocathode efficiency, the attenuation along the propagation in the optic fibers and, mainly, the limiting angle of the shifting fiber. The latter determines what fraction of photons emitted in random directions by the fiber shall remain inside.

- Photon attenuation and path increase. Photon attenuation in the shifting fiber is fitted from experimental data [2], while an exponential law is considered for the clear fiber. No losses are assumed in the fiber connection. On the other hand, a path increase probability is taken into account due to the fact that the photon is not travelling in the optical axis. We use the correction in reference [1], obtained using Monte Carlo methods.
- Photomultiplier. The quantum efficiency of the photocathode is given by a probability conversion factor. The electron signal amplification is modelled after reference [5] using a standard dynode distribution.

Typical values for those parameters are¹ :

scintillator excitation time	0.9ns
scintillator desexcitation time	2ns
Y11 fiber desexcitation time	10ns
12x12 pads photon capture and reemission probability	0.0522
4x4 pads photon capture and reemission probability	0.0725
photon attenuation length in clear fiber	4m
photocathode efficiency	0.1
photomultiplier high voltage	900V
number of dynodes	11
dynode voltage ratio	4:2:2:1:1:1:1:1:1:2:3

With this data, the typical signal shape is plotted in figure 1. This plot is in agreement with data obtained experimentally with cosmic rays on 1 MIP particles [2].

1.2 Resolution on expected data

We perform 1000 runs for every different pad sizes and pad positions in the panel (amounting to different clear fiber lengths), for the expected range of deposited energies [4]. Actual ranges shall be :

Pad sizes	: 12×12 , 4×4 cm
Clear fiber length	: 1–5 m in 0.5m steps
Deposited energy range	: 1–3 MeV in 0.1 MeV steps
	: 0.5–4 MeV in 0.5 MeV steps

¹Except for geometrical parameters already described.

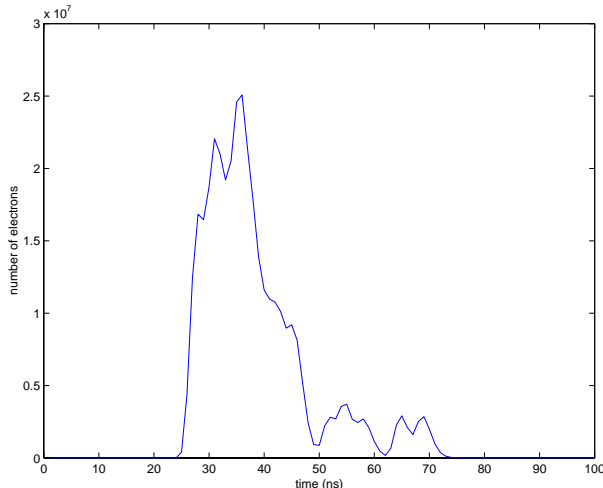


Figure 1: Sample signal for 1 MIP particle on a 4×4 cm pad with 3m of clear fiber.

For every cell and position, we simulate a calibration phase in which we use the first 250 events to select the best starting point for signal integration. We obtain an average measured charge with its corresponding standard deviation which shall be a measure of the energy resolution. In figure 2, results are shown for 4×4 cm and 12×12 cm pads with 3m of clear fiber. Charges are in electron units. Measured signal stands for the integrated charge over 25ns while total signal stands for the total charge deposited.

The average ratio of measured over total signal is 85% with a standard deviation of 15%. This average is in agreement with results ($83\% \pm 10$) in reference [2], while the standard deviation is slightly larger. This effect could be due to slightly different experimental conditions.

The dependence of the signal on the clear fiber length is far from negligible as it is illustrated in figure 3 which contains results for 4×4 cm pads. Measured signal is reduced up to 3 times.

1.3 Influence on electronics specification

Results of the previous section have to be combined with the spectrum of deposited energies for photons and electrons obtained from Geant in reference [4]. If we assume that the probability distribution of measuring charge q for a particle depositing energy E is a gaussian whose mean and standard

deviation are those obtained in the simulations, and we perform the appropriate convolution, we obtain the spectrum of measured charges. In figure 4, this spectrum is depicted for a 3m clear fiber length setting.

The 3m case is chosen because it is the one with more precise results since it corresponds to the experimental conditions from which the photoelectron count has been performed.

From the spectra, one we can infer the probability of misclassifying a photon and an electron according to different cuts which is summarised in the following table.

	Charge cut (in 10^8 electrons)	electrons	photons
4×4cm pads	1.5	0.0019	0.0379
	2.0	0.0199	0.0311
	Charge cut (in 10^8 electrons)	electrons	photons
12×12cm pads	0.7	0.0153	0.0446
	1.0	0.0736	0.0345

Two specifications are important to define the requirements of the front end electronics: input signal range and resolution. The later is related directly with photon statistics, since it limits the resolution of the detection process. From the discussion on section 1.2, an upper limit (best detector resolution) of 10 % can be taken as the required resolution of analog processing system (4 bits are enough). This is a requirement for the electronics precision and noise, non-linearity can be corrected through calibration.

The former depends on the tube high voltage, the load resistor and the number of photoelectrons. If we assume that output current of phototube is not saturating and follows the light pulse, it will consist on an exponential pulse with a decay constant (τ_d) of about 10 ns (the WLS fibre de-excitation time) and a amplitude equal to $\frac{Q}{\tau_d}$, where Q is the total amount of charge of the current pulse. If the tube is loaded by a resistor (R_L) and a parasitic capacitance (C_{par} of about 1 pF), the circuit time constant has to be much lower than the signal decay constant to work in current pulse mode ($R_L \times C_{par} \ll \tau_d$). Hence, a load resistor of the order of 100 Ω will be chosen. In that case the voltage signal on the load resistor can be approximated by an exponential pulse of decay time constant τ_d and an amplitude $\frac{Q}{\tau_d} \times R_L$. The maximum voltage amplitude is achieved when the tube high voltage is 900 V, and it is (for 35 photoelectrons) about 50 mV. When tube is operated at 600 V it is 50 μ V.

Taking into account the variation between channel gain in the multianode photomultiplier (MAPMT) R5900-M64 of Hamamatsu (up to factor 5), the following requirements are specified:

- Input signal range: from 0 to 250 mV.
- Input voltage noise for the front end electronics should be $5 \mu\text{V}$ r.m.s.
- Precision: 10 %.
- Resolution: 4 bits. Threshold code: 4 bits (res.) + 3 bits to cover MAPMT gain fluctuations.

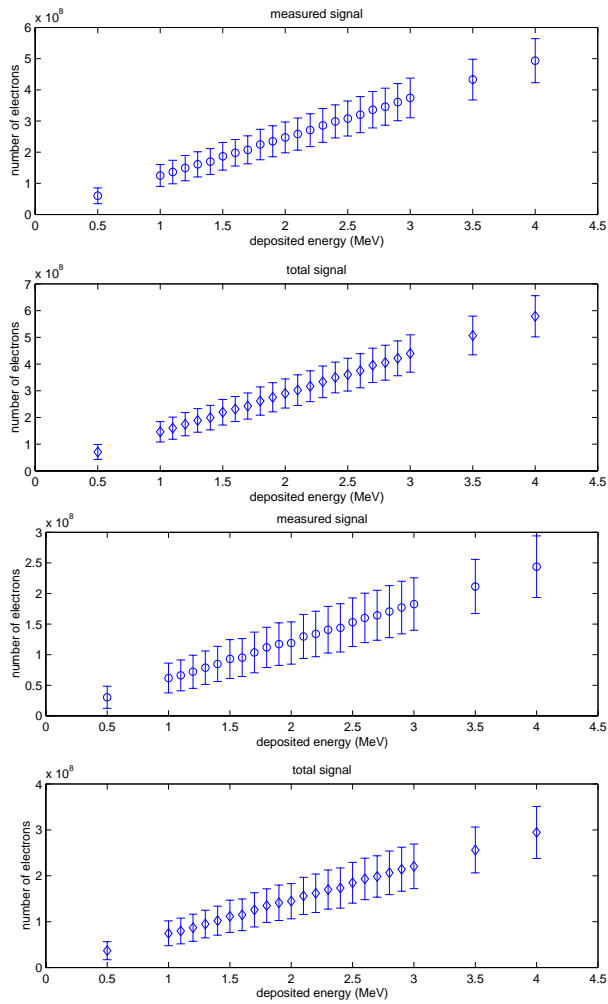


Figure 2: Influence of deposited energy in the measured and total signal for 4x4cm pads (top) and 12x12cm pads (bottom). The mean and the standard deviation of PMT output signal spectrum are plotted.

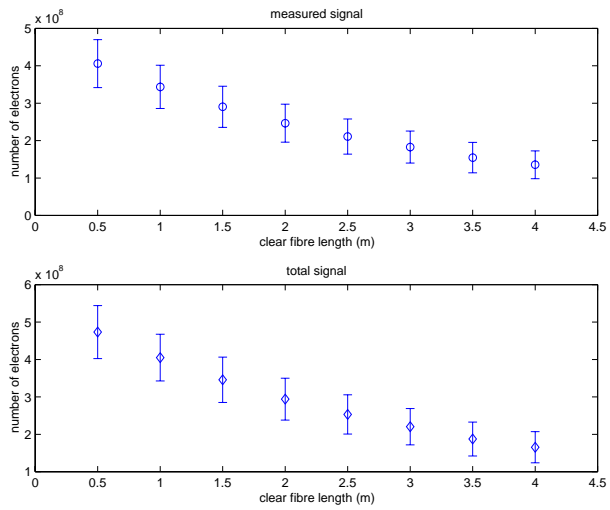


Figure 3: Influence of clear fiber length in the measured and total signal for 4×4 cm pads. The mean and the standard deviation of PMT output signal spectrum are plotted.

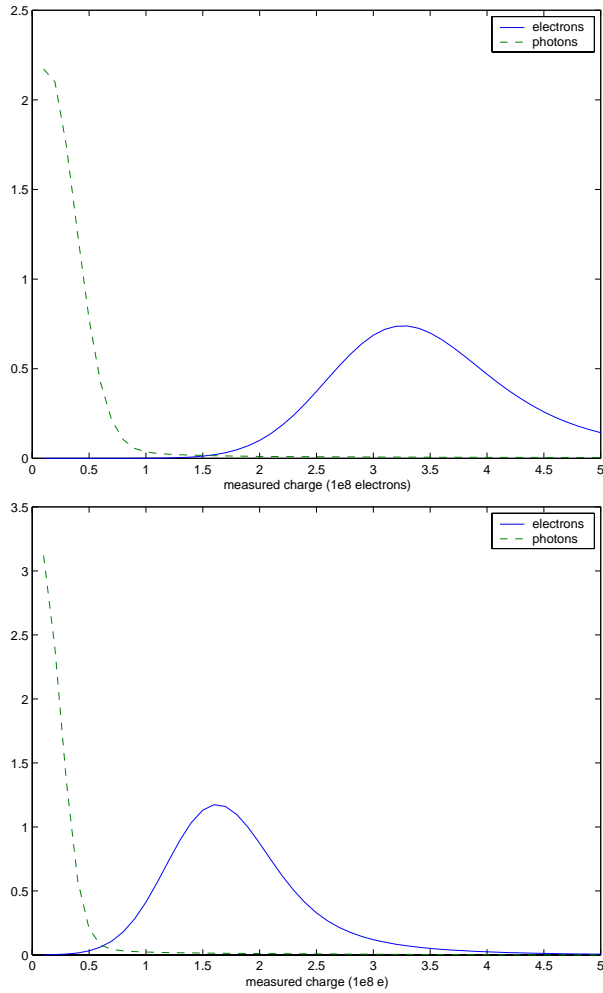


Figure 4: Measured charge spectrum for $4\times 4\text{cm}$ pads (top) and $12\times 12\text{cm}$ pads (bottom).

2 Front-end discriminator ASIC design.

This sections describes the architecture and implementation of the first ASIC prototype designed to distinguish between the signal produced by a charged and a non charged particle on a SPD cell (see [4]), therefore it is a discriminator circuit.

This circuit will be implemented with an ASIC due to the following reasons:

- Integration. The SPD front-end manages more than 5000 channels, for this reason the area of each channel must be minimum.
- Signal speed. The frequency of the signals in the experiment (40MHz) requires a fast analogue design, which can be performed with BiCMOS.
- Power consumption. The integrated solution will operate with less power consumption compared with discrete board solutions.

We have decided to use BiCMOS technology because it has the potential to overcome the inherent drawbacks of the MOS device (lack of high speed capability and precision) as well as the specific shortcomings of the bipolar device (no VLSI capability due to power and area restrictions). The advantages of BiCMOS in analogue circuits include not only an improvement in speed or band-width but also a reduction of precision problems such as parameter fluctuations and device degradation. A standard 0.8 μm BiCMOS technology from AMS has been selected as a target technology. This technology is easy to access through MPW services at competitive prices for prototype integration and fulfills the requirements of our design. Low volume production is also possible. For the moment, we plan to include in each ASIC 16 complete channels (figure 5), but further tests are needed to verify this point.

2.1 Analogue processing chain

In order to design properly the discriminator we must take into account the statistical properties of the signal, related to the nature of a scintillator detector and the de-excitation time of the WLS fibre, which follows an exponential probability distribution with a time constant of about 10 ns. On average about the 85% of total signal is integrated in a bunch crossing period

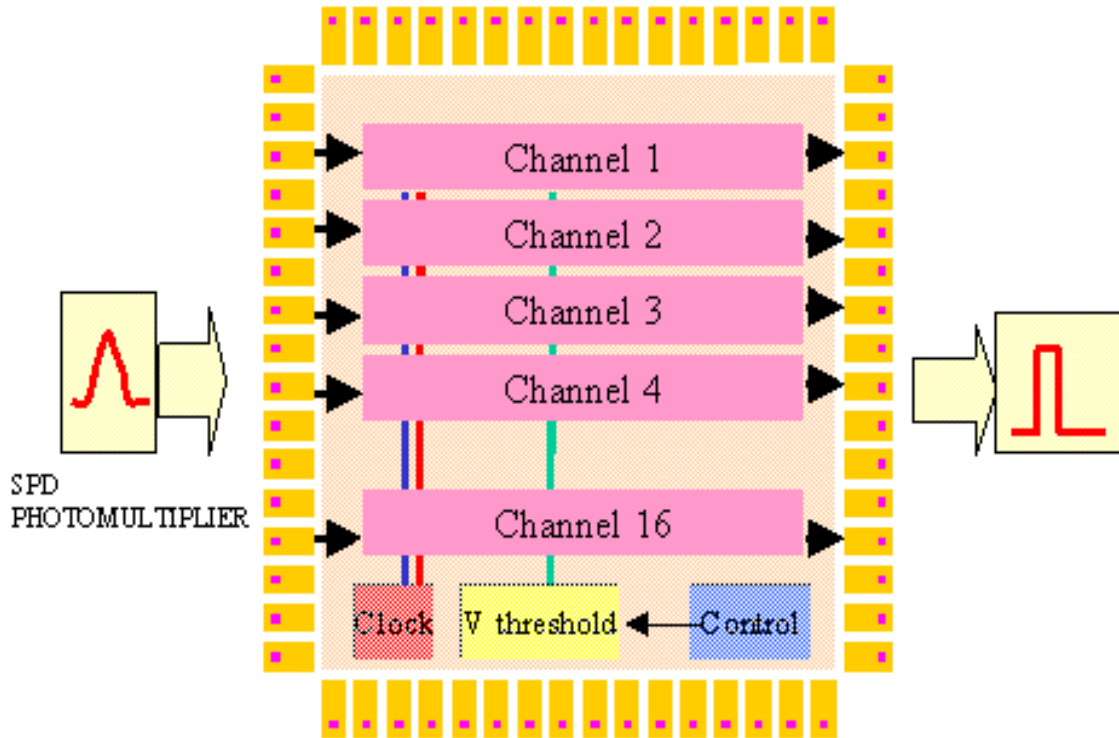


Figure 5: Floorplan of the front-end ASIC.

(25 ns). Typically a 14% is integrated during the following bunch crossing. However, because of fluctuations in the position of the light conversion in the fiber and in the photoelectron statistics the fraction of integrated signal in the first period can vary about a $\pm 15\%$ and about a $\pm 35\%$ in the next period for a 4 cm side cell (see [1] and discussion on first section of this note). Therefore, the mean signal lasts more than the maximum integration time allowed: 25 ns.

Moreover, the probability to have two interesting consecutive signals is not negligible, being of the order of 7 % on the central region.

This has two main consequences on the electronic design:

1. A dual-path architecture is needed in order to do not have any dead time due to integration reset.
2. Pile-up correction. Pile-up means that part of the signal of the event n is detected on the event $n+1$, and there is no way to distinguish from

the signal detected on the event $n+1$. Although it can not be avoided a statistical compensation is possible by subtracting a fraction of the integral signal of the event n from the integral signal on event $n+1$.

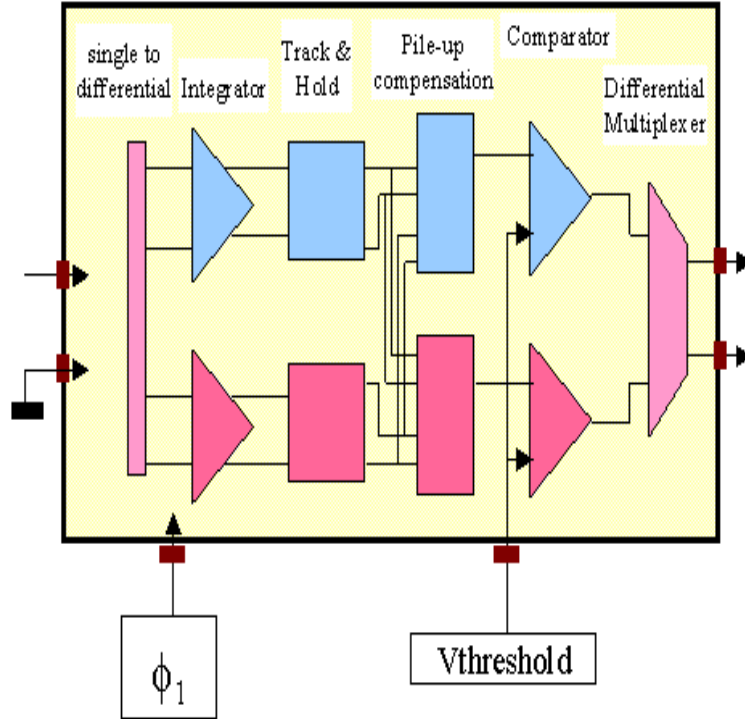


Figure 6: Very front-end detailed design. A dual channel architecture is needed because the probability to have two interesting consecutive events is not negligible. In order to perform calibration and to correct the gain between different PMT channels, the threshold of each front-end channel will be programmable.

The proposed structure of the discriminator is shown in figure 6. In order to reduce noise the design has a differential architecture. Because of the jitter of the input signal and its non-reproducible shape, the signal coming from the photomultiplier has to be integrated rather than just considering its maximum value. So, the input device of the discriminator is an integrator circuit.

Each path of the discriminator is controlled by an opposite clock phase of period 50ns (twice bunch crossing period). Possible pile-up is corrected then by subtracting a fraction ($\sim 17\%$) of the integrated signal in the clock-cycle n from the signal being integrated in the clock-cycle $n+1$. To do this, the signal integrated in the clock-cycle n has to be stored in a track and hold. After the subtraction has been performed, the signal is compared with a threshold value established in the comparator. Finally, after the comparators, a multiplexer is added to select the path from which the signal is read in this channel. Different versions of the integrator (based on an alternative differential amplifier), track and hold and subtractor were designed for the first prototype submitted to the AMS MPW run on March 17, 2000.

The schematics at transistor level of these modules are presented in fig. 7. To avoid the signal coming from the integrator during reset to be sampled by the track and hold, the track and hold and the subsequent blocks are controlled by a clock, which is 2.5ns advanced with respect to integration clock. All the blocks of the circuit are biased between +2.5V and -2.5V. The channel will be completed with a single ended mode to differential mode converter block at the input of the circuit.

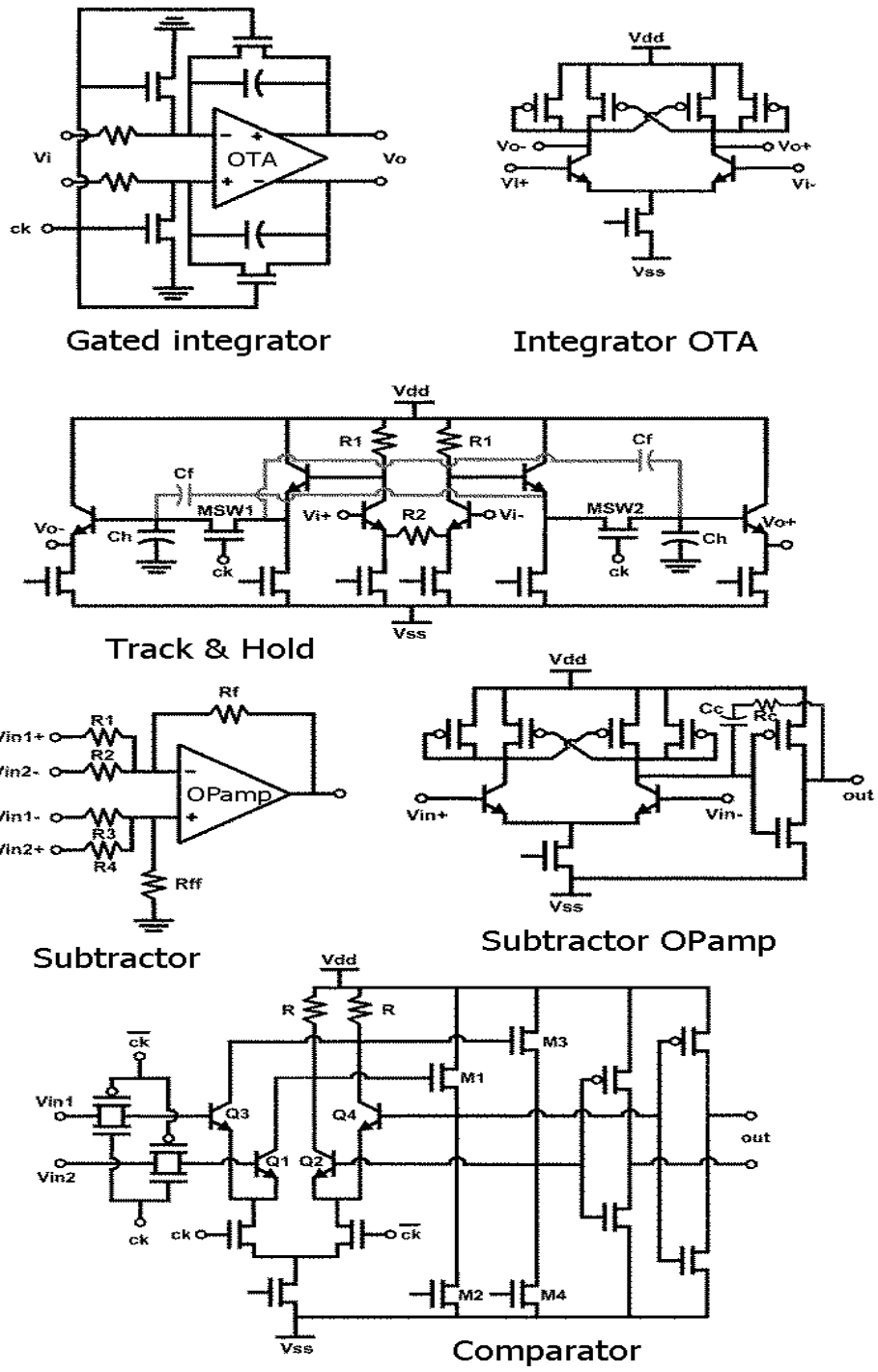


Figure 7: Schematics of the building blocks of the fully synchronous discriminator.

2.2 Electrical Simulation

The complete circuit has been simulated using Spectre as electrical simulator. Figure 8 shows an example of the operation of the discriminator circuit. *Clock* signal is the 20 MHz (half the bunch crossing frequency) channel clock which gates the integrators for 25 ns and controls the internal switches. When *Clock* is high the sequence of signal processing works as follows:

- Integrator 1 is integrating the input signal and integrator 2 is discharging its feedback capacitors.
- Track & hold 1 follows *Integrator 1* signal and Track & hold 2 holds *Integrator 2* signal.
- The output signal of subtractor 1 (*sum 1*) is the input signal of comparator 1, and the value of this signal is: "*Track & hold 1*" - 0.17 * "*Track & hold 2*".
- Comparator 1 compares its input signal (*sum 1*) with *Threshold 1*, giving at the output (*Comparator 1*) the transient result of the comparison which will be latched on the next *Clock* period (when this clock falls to the low level).
- Comparator 2 is in "latch" operation holding at his output the result of the previous comparison, which is transmitted to the output of the channel through the multiplexer.

A symmetric situation occurs when *Clock* is low.

On this simulation we combine two signals that corresponds to the opposite tails of the statistical fluctuation of the PMT signal. The conditions to define PMT signal are: 1 MIP signal is equivalent to about 35 photoelectrons, the high voltage is set to 900 V and the load resistor at the output of the tube is 100Ω. These signals are approximated by exponential pulses of 50 mV and 10 mV with a time constant of about 12 ns. Threshold is set to detect signals of the smallest amplitude. Three different situations are simulated:

1. At $t=25$ ns (period² 2), a pulse of maximum amplitude is integrated. After following all the processing chain a high level on the comparator 1

²"Period" is used to name a bunch crossing period (25 ns), half a period of *Clock* signal.

output (period 3) indicates that a charged particle has been detected. Therefore, the delay of the processing chain is one cycle. Although the amplitude of the tail of the signal at period 3 is high (*Integrator 2* signal at period 3) the compensation of 17 % of the signal hold at Track & Hold 1 output avoids that input Comparator 2 signal (*Sum 2* signal at period 3) exceeds *Threshold 2*. The tail is not taken as new 1 MIP signal although its integral value (*Integrator 2* signal at period 3) is of the same order of the integral (*Integrator 2* signal at period 13) of the 10 mV signal that has been used to adjust Thresholds.

2. At $t=125$ ns (period 6) we have a 50 mV amplitude pulse and on the next bunch crossing (period 7) (half of *Clock* signal period) a pulse of 10 mV amplitude is overlapped to the tail of the large one. Both signals are detected: the big one at the Comparator 1 output at period 7 and the small one at the Comparator 2 output at period 8.
3. At $t=300$ ns (period 13) a 10 mV small amplitude pulse arrives and it is detected.

To be efficient this compensation mechanism needs a precise estimation of the mean percentage of signal integrated in 25 ns ($\bar{\alpha}$). Moreover, studies are needed to determine wrong discriminations as a function of the statistical fluctuation ($\delta\alpha$) of this value, which can lead to the identification of the tail of "big" signal as a small signal or to loss "small" signals coming just after a "big" signals with α much bigger than $\bar{\alpha}$.

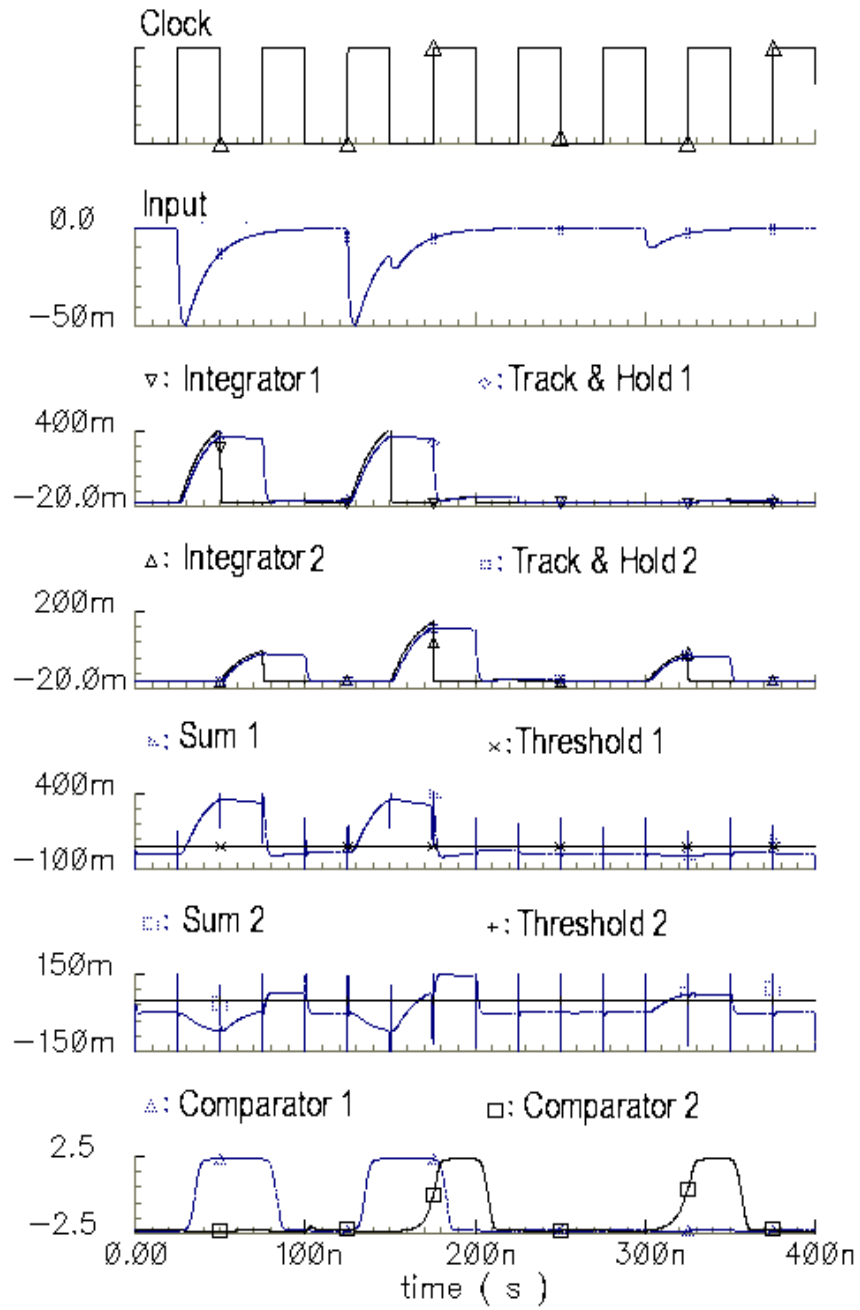


Figure 8: Simulation results of the discriminator blocks. Processing steps for three possible events.

2.3 Thresholds setting and controls

As a consequence of the large dispersion in the gain (between 2-5) of each channel of the photomultipliers, is necessary to tune the PMT load resistor to adjust the gain and to introduce the possibility to adjust the threshold used in each discriminator, thus allowing a calibration of every detector channel. The proposed solution, presented in Fig. 9, intends to avoid increasing the ASIC pin count or the board complexity.

A global threshold voltage is introduced in each PCB, this signal will be used to adjust the voltage reference of an in-chip Digital-to-Analog converter (DAC), this reference will depend on the gain determined by the PMT high voltage. The function of the DAC is to split the global threshold voltage in different levels. The level of several channels will be stored in an external memory (EEPROM or Flash memory) and introduced in each ASIC using a serial port when it is needed. As has been exposed on section 1, 4 bits seems to be enough for the resolution threshold coding and does not limit the maximum energy resolution achievable at SPD, which has been estimated to be around 10 %. Three additional bits are needed to cover the extension on signal dynamic range caused by the fluctuation of channel gain on MAPMT, therefore threshold will be coded in 7-bit word.

2.4 Test signal

Since the PMT signal is single ended by nature, each channel will include as first stage, a single to differential block. This leads to a reduction of the number of input pins and also the possibility of introducing a test signal in order to check the status of the different channels in a given IC (figure 10). Although this is the baseline solution, the possibility of using a differential input is also being studied, to reduce the possible common mode noise and common mode pick-up noise at PCB level. Further tests are needed.

3 System design

3.1 General design according to specifications

The read out system is functionally organized in processing units. Each unit comprises (see figure 11): the photomultiplier to convert scintillation light to charge, the analog processing chain integrated into an ASIC (see previous

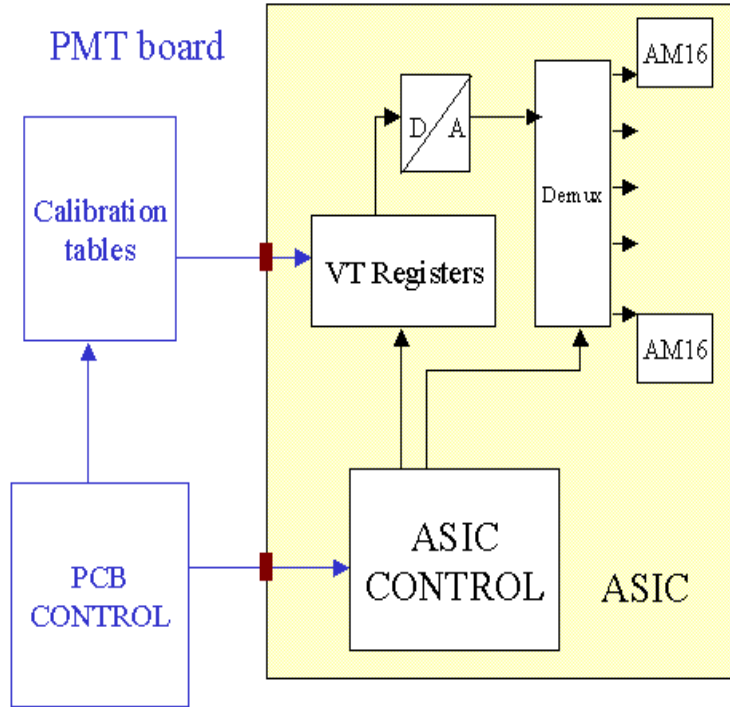


Figure 9: Individual threshold control block. The threshold of every channel is set according to the on-line calibration of the channel. Once it is calculated it is written on the memory (calibration tables) and transmitted to the front-end ASIC. The threshold of each channel is latched on a register (Vt register), it is converted to an analog value and this value is stored as the reference of the discriminator.

section), a delay unit to synchronize the gated integration clock (named ϕ_1) with PMT signal, a control unit needed to manage calibration, synchronization and monitoring procedures, and field bus interface to communicate the front-end electronics with the Experiment Control System (ECS).

The control unit will be the responsible of passing the correct thresholds to the ASIC and synchronize the front end system clock. It will also monitor board temperature, voltage and current consumption to assure a correct operation. This control unit will communicate with the ECS through a field bus. The control unit will also generate a test signal to check the right functionality of the ASIC. This test signal will be redirected to the 16 channels

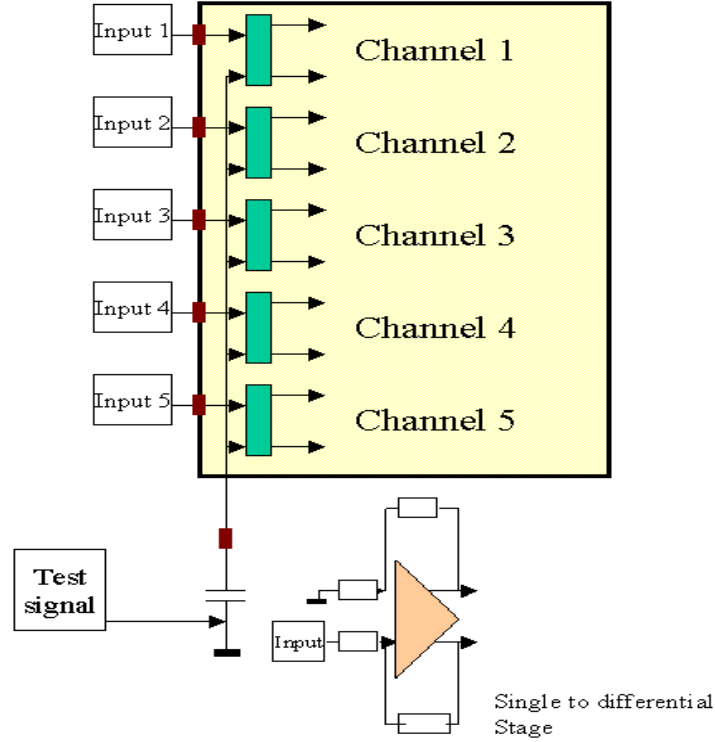


Figure 10: An input block will be used to convert the single ended input signal to differential signal. This module will also be used in order to perform an individual test of each channel.

in the ASIC.

3.2 Bunch crossing synchronization

The integration of the photomultiplier signal is controlled by the clock ϕ_1 in figure 6 (obtained from the bunch crossing clock at the PS front end card using the TTCRx chip). The leading and trailing edges of this clocks start the integration on the upper and lower integrators, respectively, of the dual channel structure (see section 2). Therefore, the output signal of the photomultiplier must be in phase with ϕ_1 , this is the so-called bunch crossing phase synchronization. In order to align the signal and the integration clock a delay unit will allow the adjustment of the phase of ϕ_1 for all the channels corresponding to one photomultiplier (see figure 11). This solution implies

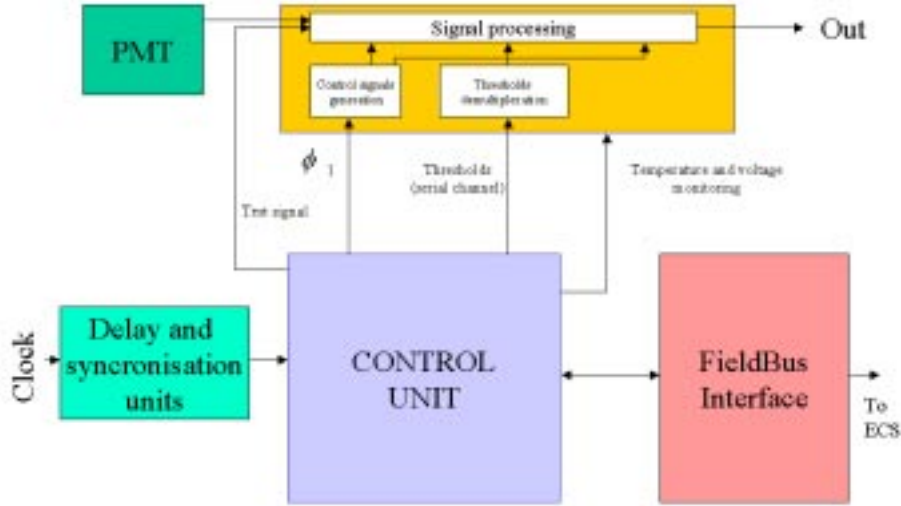


Figure 11: General synoptic for the SPD electronics. This graph is a functional diagram of the SPD electronics. We will need a Supervisor unit to manage about 4 PMT boards. The field bus interface communicates with ECS. To synchronize the clock we will have several delay blocks to generate the needed phase (ϕ_1) in order to integrate the PMT signal in the ASIC.

that the signals of all the channels of a given phototube must be in phase, and thus the length of all optical fibers must be the same. It seems feasible to adjust the delay for the integration clock of each photomultiplier optimizing the response efficiency as a function of this delay. For this reason, and also to adjust threshold value, it is necessary to acquire and save the output information of the SPD together with the PS data.

Several delay units fulfill the requirements for this application: range from 0 to 24 ns and *time resolution* ≤ 1 ns. Some examples of these units are:

- PHOS4 (Cern Microelectronic Group). It is a 4-channel delay generation ASIC with 1 ns resolution. It is programmed through a I2C interface. A possible drawback will be its cost if it is produced finally only on DMILL technology.

- CY7B991V (Cypress Semiconductor). It is a 3.3V RoboClock low voltage programmable skew clock buffer with LVTTTL outputs capable of driving 50 ohms terminated lines. It has four pairs of independently controlled outputs. The user can create output to output delay of up to ± 12 time units (steps from 0.7 to 1.5 ns). One may need to cascade two delay units in order to create delays of 24 ns.
- DS1021 (Dallas Semiconductors). Programmable 8-bit silicon delay line. Models with 0.25 ns and 0.5 ns steps. TTL/CMOS compatible. Only one channel on each circuit.
- PDU18F (Data Delay Devices). Programmable 8-bit delay line. The incremental delay can range from 0.5 ns through 10ns. The address is not latched and must remain asserted during the operation, thus a interface should be designed. Only one channel per circuit.

This component will be common to all the different calorimeter front end cards (and perhaps to other LHCb detectors). A common evaluation and choice will be done.

3.3 Output data synchronization on PS front end card

A phase and period synchronization is needed for SPD data. The first one because front end boards clocks that control integration are not in phase. The second one provokes that the same data period will correspond to different bunch crossing periods for channels of different photomultipliers due to the difference on fiber length and data link between SPD and electronics crates. To perform data synchronization, the SPD output bit stream will be time-aligned at the PS front end card adding wait cycles on the appropriate channels. To re-phase data for PS front board clock several solutions are possible. Since it is a problem for all the front end links a common solution should be adopted. An extra pair of cables are reserved on the data link between SPD and PS in case it is needed to send the local clock of the SPD "PMT board" to re-phase properly data at the PS card.

3.4 ECS interface and functions

The main functions that the Experiment Control System should perform on the SPD front end electronics are:

- Distribute channel threshold value.
- Program delay units for the bunch crossing synchronization.
- Read any parameter that controls the analog processing performance: thresholds values, possible monitoring channels, clock synchronization parameters,...
- Monitor the parameters of the front end boards: voltage, current, temperature.

Various solution exist for the front end board intercommunication and connection with ECS. They are studied in the front-end and ECS LHCb working groups, and a common solution is expected to be chosen by mid 2001, at least for the calorimeter groups.

3.5 Board structure and sizes

We have studied several options to distribute the parts listed in the last section. First of all, we thought in only one board containing everything. The problem was that the complexity of the board was high: we needed a board with many layers, the cost was high and we had to implement one control unit for each PMT.

Therefore, we decided to split the functional design in two physical boards. We wanted to separate the PMT and the 4 ASICs from the control unit, the bus interface and the delay lines. This allows us to use one control unit board for more than one PMT board. Hence, smaller number of components are needed, and the complexity of the boards and the cost are decreased.

Let us call "PMT board" the board with the PMT, the 4 ASICs and the corresponding connectors for the outputs, and "Supervisor board" the board with the control unit, the delay lines and the bus interface. We will have one PMT (64 channels) and 4 ASICs of 16 channels in each "PMT board". We can use one supervisor board to serve more than one PMT board. Each supervisor will control around 4 "PMT boards" by means of point to point link.

In the "PMT board", a connection is needed to the PS front end card (where data is joined to PS trigger information) for the 64 channels. For this purpose, we will use a 17 pairs connectors for twisted flat cable, therefore we will need 4 of them in each board. The sizes of these connectors are smaller

than 45 mm x 8 mm each. We foresee a 25 mm x 25 mm socket for the ASICS and 30 mm x 30 mm for the PMT (assembly H7546).

To fit the mechanics design of SPD and PS (see [6]) we will place the PMT on the reverse side of where the connectors will be placed. We can see in figure 12 which will be the final disposition of the components and the estimated sizes of the board in millimeters.

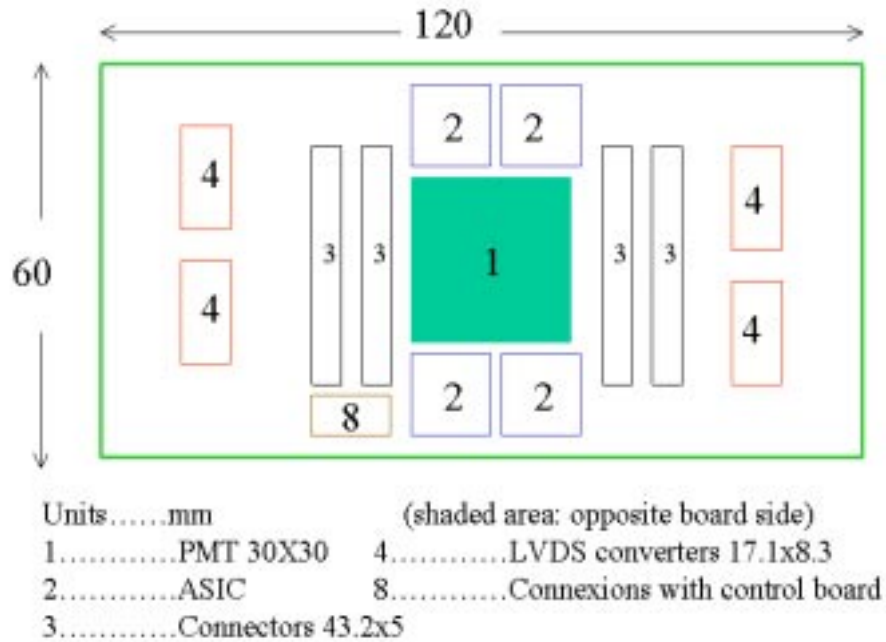


Figure 12: Front-End PMT boards distribution. There are the 4 connectors to communicate with preshower and one more to connect alimentation and other signals with the Supervisor board. There are 4 chips to convert the CMOS level of the 64 channels outputs to LVDS signal levels. The sizes of these boards should be 12 cm x 6 cm. The PMT and the connectors will be on the opposite sides of the board.

Figure 13 outlines the disposition of the different parts of the supervisor board. It is too early to talk about specific components yet. The PMT boards and the supervisor boards will be properly connected through the board part 8 as shown in figures 12 and 13.

The possibility of using the multiplexer facility of Low Voltage Differential Signaling (LVDS) digital links is studied to reduce the number on cable pairs

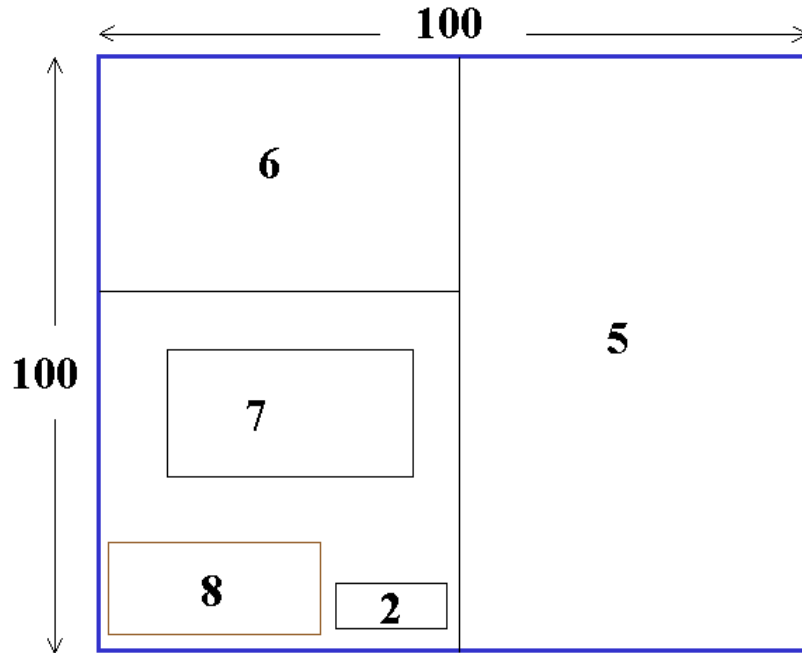
needed to transmit data to PS front end cards. It seems possible to reach about a factor 6 of reduction, but commercial links receivers (like the 16-channel SN75LVDS387 of Texas) should be included on PS front end card in this case.

4 Acknowledgement

The idea on the dual and synchronous analog processing architecture was proposed by our LPC (Clermont) collaborators. We wish to thank the contribution and comments of Alain Falvard, Jacques Lecoq, Pascal Perret, Cyrille Trouilleau of LPC, Olivier Callot, Jacques Lenfrancois, Vanesa Tocut of LAL (Orsay) and Evgueni Goutchine of INR (Moscow).

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Units.....mm

2...Power supply 5...Control Unit

7...Clock delays 8...Connection with PMT board

6...Field bus interface

Figure 13: Supervisor board distribution. It will include a bus interface to communicate with ECS and a control unit that will be used to manage more than one PMT board, together with the programmable delay units to synchronize the clocks of each PMT board.